Mini in Bikini: a TTL university made Computer at Universidad Nacional del Sur*

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Abstract. In this paper we present the design and implementation of a mini computer at Universidad Nacional del Sur (Bahía Blanca, Argentina) in the first years of 1970's. The name of the computer was "Mini in Bikini". The project was done by a group of Electrical Engineering students guided by Prof. Santos. A short review on the political and economic context is presented together with the computer engineering and science development at the moment of the project conception. The technical details of this mini computer are presented together with an emulator developed by Prof. del Castillo many years later.

Keywords: Computer history · Mini Computers · University computers · Education with computers.

1 Historical context in Argentina

The period that extended between the mid-50s and the first half of the 70s was one of political effervescence and social mobilization in Argentina. In this context, the civil and military governments and the business community projected Bahía Blanca as a pole of economic development. The port, railway, road and air infrastructure, together with commercial and industrial development, positioned the town as the center of an area of influence that brought together fifteen districts of the province of Buenos Aires with projection over the provinces of La Pampa, Río Negro and Neuquén. The number of inhabitants of the district went from 126,669 in 1960 to 182,158 in 1970 [1]. Half of them were part of the middle income sectors with aspirations for social advancement through education, in particular by following a university career.

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After the coup d'état that overthrew President Juan Domingo Perón in 1955, there were interventions by the authorities in the field of higher education. That was the case of the Instituto Tecnológico del Sur of Bahía Blanca, which became a decentralized entity until it was granted university status. The new interventor, with support from various social sectors, decided to pressure the government through a strike. As a consequence, by means of decree-law No. 154, the Universidad Nacional del Sur (UNS) was created.

With the Peronist party banned, Arturo Frondizi won the elections in 1958. He had a developmental project to transform the country, which included the opening of higher education entities outside the orbit of the State for technical training. This provoked the controversy called "secular or free" [2], about the equality between state and private universities in terms of vocational training or the preeminence of the former, which extended to the UNS. The president was overthrown by a new military coup in 1962, whose political repercussions were echoed in the Bahia university community. The following year, with Peronism banned, there was a return to democracy through elections in which the formula headed by Arturo Illia was elected. During all those years, despite the turbulent national reality, the fragmentation of the student movement, the union conflict of non-teaching personnel and the budgetary and building problems, the UNS had consolidated itself by extending its academic ties and its regional projection, and had been the beneficiary of important grants [3].

In 1966, faced with the deterioration of the authority of the national government and the possibility of a return of Peronism or the advance of leftist revolutionary tendencies, the president was overthrown by a military coup led by Juan Carlos Onganía. Republicanism gave way to corporatism and a repressive model was implemented that affected sindicalism, political parties, and student movements. This promoted the political radicalization of youth groups, leading to the integration of the first armed organizations. In this context, universities were intervened and academic autonomy was put to an end. This implied the annulment of tripartite government and student participation in university politics. The majority of national universities rose up in open opposition to the government, leading to the resignations of authorities and professors. At the UNS, the rejection was manifested through statements by teachers, groups of graduates and students, and restrictive measures on political activity were quickly implemented. The student agitation did not wait, generating surveillance, incidents, arrests, injuries and raids that affected those suspected of being communists and subversives. Despite this, in the material aspect, the institution's prospects towards the end of the sixties were promising due to the acquisition of land, advances in infrastructure and modernization [3].

Onganía remained in the presidency until 1970, when General Roberto M. Levingston replaced him to be removed in turn by General Alejandro A. Lanusse in 1971, the year in which there was an escalation of violence that included the university communities. Growing discontent forced the military government to seek an electoral solution by allowing Perón's return, but banning his candidacy. In 1973 an election was held in which the formula headed by Héctor Cámpora

triumphed. At the beginning of a new institutional stage, some professors and UNS authorities presented their resignations. Shortly thereafter, the president resigned with the purpose of calling for a new election, which would result in Perón as the winner. In this context, University Law No. 20,654 was passed, which aimed at the normalization of higher education institutions.

The death of the president in 1974 produced an escalation of violence that was accompanied by an economic and political crisis. The confrontation between the most combative sectors of the left and the right -Peronist and non-Peronist- and the increase in government policies impacted university institutional life [3]. The actions of armed organizations and repression by the Armed Forces increased. At the same time, Triple A paramilitary gangs, created by José López Rega, kidnapped and murdered opponents, including university students linked to Marxism. The arrests of students and the dismissals of teachers and non-teachers multiplied. In 1974 Jesús "el Negrito" García was kidnapped and murdered and in 1975 the engineering student David "Watu" Cilleruelo was murdered in the hallways of the UNS by a member of the custody of the interventor, Professor Remus Tetu.

In 1976, another military coup deposed María Estela Martínez. The de facto regime calling itself the "National Reorganization Process" promoted State terrorism and the violation of public and individual freedoms as the central axis of its management. The repressive climate was particularly intense in Bahía Blanca, where the presence of important military units, both from the Navy and the Army, accentuated the terrorist action at the same time that the presence of the journalistic multimedia led by La Nueva Provincia legitimized the government's actions in the political and economic level [4]. At universities, a control and surveillance device was implemented over the administrative, teaching and student staff, aimed at neutralizing the sectors classified as subversive, which generated a latent and effective threat of arrest, kidnapping, torture, disappearance or death. In addition, the operation of student centers was prohibited, disciplinary regulations were tightened, study plans were changed, programs and bibliography were censored, restrictions on entry into social science courses were established, and fees were introduced [5].

The democratic restoration would only occur in 1983 and would lead to the beginning of normalization processes in Argentine universities, including the UNS. Since its creation until that date, it had established itself as the most important educational and cultural institution in the region of influence of Bahía Blanca [3]. Furthermore, despite the difficulties that his institutional life had faced, it had integrated with the environment and its teachers had generated academic contacts with national and foreign peers.

1.1 Computer Science and Engineering first years

Starting in 1956, an intense modernization process began at Universidad de Buenos Aires (UBA), at the epicenter of which was the School of Exact and Natural Sciences (FCEN). In this context, at the end of 1957, the directory

council of FCEN headed by Dean Rolando Garcia resolved to create an institute dedicated to the study of computers "Instituto de Cálculo" (IC) and seek financing to provide it with a computer. To face the project, a commission of 3 members was formed, among which was Manuel Sadosky, whose imprint marked the entire process. Already in 1958, after obtaining a financial support from the brand new Consejo Nacional de Investigaciones Científicas y Técnicas (CONICET), a tender was held for the purchase of a computer. The result was the acquisition of a Ferranti Mercury equipment that arrived in Buenos Aires in November 1960 and was fully operational by May of the following year. In this way, academic computing began in the country. Shortly after, in 1963, the first computer science related undergraduate career was launched at the same faculty. At the time, computers were very large and required special cabinets to hold them. Their use was not generalized and accessing one was a kind of infrequent luxury [6][4].

At the same time, at Universidad Nacional del Sur there was a group of researchers working first with a "Seminario de Computadoras" and later in a project to build a national electronic computer, CEUNS [7], under the supervision of Prof. Jorge Santos. Both groups have a strong relationship and interaction. For example, the machine language of CEUNS was developed by Prof. Victoria Bajar that was working with Prof. Sadosky at UBA. Even though CEUNS was not finally built, the project produced several results that were published in journals and conferences of the time [8–11]. This project was important for the development and consolidation of the computer engineering research group and the most relevant immediate antecedent for the realization of the Mini in Bikini ten years later, also under the supervision of Prof. Jorge Santos. This project took place between 1973 and 1975. Later, different students complemented the computer by adding memory modules in 1976 and 1978.

The aforementioned military coup in 1966 led by General Onganía was extremely detrimental to all science in Argentina, but particularly to a new area that had not yet been developed either in Argentina or in the world. Many professors resigned from their positions and emigrated to other countries, mainly Uruguay, Venezuela, Brazil, France, the United States and the United Kingdom, in protest at the suspension of university autonomy. Mass resignations led to the destruction of research groups. These resignations mostly took part at Universidad de Buenos Aires. At Universidad Nacional del Sur things were different and the research groups continued working since the rector Aziz Ur Rahman agreed to continue in his position depending on the dictatorial government. As Patricia Orbe points out: "Supported by a sector of the local university population, Dr. Rahman directed the destinies of the UNS together with the Directors of Departments as administrators dependent on the National Executive Branch. There were some resignations of teachers from their positions in repudiation of the new situation, but at the University in Bahia Blanca, the intervention did not have the magnitude that it had in other houses of higher education" [3]. However, there were actions to repudiate the military coup by the student move-

[4] Thanks Prof. Raul Carnota for the historical context at UBA.

ment, which demanded autonomy and university co-government. In mid-1967, maintaining that he had fulfilled the purpose of keeping order, Rahman resigned from his position and was replaced by Manuel Eduardo Gómez Vara as intervener appointed by the dictatorship.

While in 1966 the professors resigned in 1976 they were fired. The impact was extremely hard and needed a long time to recover. For example, it was not until the return of democracy that universities were in conditions to create Computer Science academic departments, at Universidad de Buenos Aires in 1985 [12] and at Universidad Nacional del Sur in 1994 [13].

2 A short review on the evolution of computers

In 1948, the University of Manchester, ran for the first time a stored-program electronic computer. It was designed and developed by Frederic C. Williams, Tom Kilburn, and Geoff Tootill. The computer was built to prove the performance of the tube memory designed by Williams but in the end proved that a general purpose stored-program computer was feasible. The first program to be ran was written by Alan Turing to calculate the highest proper divisor of 2^{18} by testing every integer from 2^{18} downwards. It took about 52 minutes to arrive to the answer. The machine only count with 7 instructions and was named Manchester Baby [14]. This computer evolved and was eventually produced as Ferranti Mark I which was the first commercial general purpose computer [15].

In 1964, IBM announced the IBM System/360 mainframe computer. The idea behind it was that software would not need to be changed each time the computer was replaced. For the first time the concepts of software and hardware were split. System/360 was used both in academic and commercial activities [16]. Companies could buy a small system and enlarge it later without having to rewrite the software. The System/360 became a kind of standard at the time and this pushed the creation of computer careers around the world.

Mini computers were thought as a way to introduce computers for academic and commercial purposes but without the requirements of mainframes computers. In [17] there is a timeline with the evolution of mini computers and the concept definition. It is stated: "*It is intended for a single user or small group of users, it is physically small (at least compared to a mainframe system), and sells for a fraction of the price of a mainframe (often at least an order of magnitude less).*"

As stated, a computer was a large machine deployed at a special place with several terminals. Its use was exclusive and only granted when it was required. Nevertheless, the idea of using small computers involved with industrial processes was present. Following the fashion of mini skirts or mini Cooper automobile, in the early sixties the mini computers appeared as a possibility. The first ones were DEC PDP-1 and the CDC 160-A but it was not until 1970 that the term mini computer was used with the PDP-8/e. Mini computers evolved as new requirements were demanded until eventually this kind of computers weighted

hundreds of kilograms and drew considerable power. In this scenario super mini computers were introduced.

In this context, the Computer Automation company produced a series of mini computers that started with PDC 404 and PDC 808 which stands for Programmed Digital Controllers. The last one was announced around July 1969. Its purpose was to provide control, monitoring and data logging applications. It provided 4 KB of core memory that was expandable up to 16 KB. It was designed using DTL logic gates. Computer Automation kept working in the development of these kind of machines and in 1971 it introduced Alpha 8 and Alpha 16 for processors of 8 and 16 bits respectively using DTL and TTL gates. The memory options were 4KB and 8KB and in some cases came with 16 KB magnetic core full cards. The input interface had a variety of options like a paper tape through a special board called the utility controller that was able to drive other peripherals like printers. There was a magnetic tape controller too. The programmer console had a row of toggle switches for data entry and boostrap routines [18]. Computer Automation named the Alpha 16 as Naked Mini. In the flyer of the computer they stated [18]:"*we had some simple, yet very ambitious goals. We wanted to offer a minicomputer that is -above all -easy to use. Even more, it has to be dependable and very low in cost. With no sacrifice in computer power*"

Although Argentina was in the middle of a political and economic crisis, at Universidad Nacional del Sur the incentive to be part of the developing technology that would finally change the way in which we live today was intact. It was in this context that Prof. Jorge Santos led a group of students in the design and implementation of a mini computer to be used within the laboratory as a prototype and to be developed as a national computer in order to replace what at that moment was imported. The result was the Mini in Bikini, supposedly a bit better than the mentioned Naked Mini. The Mini in Bikini project was oriented to the teaching of processor architectures and its hardware operation. Software was complimentary and just simple programs were prepared.

Contribution: In this paper, we present the main technological aspects of the Mini in Bikini computer: its architecture and programming language. An emulator is presented with which the Mini in Bikini can have a second life.

Organization: The rest of the paper is organized in the following way. In Section 3 the Mini is described in all its components. Section 4 presents the emulator and Section 5 provides the conclusions and future work.

3 Mini in Bikini

The mini computer project was developed by three students: Lidia Luisoni, Ricardo Barrios and Néstor González. Each one was in charge of a part of the computer's architecture guided by Prof. Jorge Santos. Later Anibal Gil and Rodolfo del Castillo added RAM memory to the computer making it fully operational under the supervision of Mg. Jorge Ardenghi and Eng. Enrrique Arroyo.

The general aim of the project was to provide a mini computer for its use within the industry, commerce and scientific research. This project was aligned

to the conclusions of the "Mesa Redonda de Política Nacional de Computación" [19] that took place in September 1973. The objective was also aligned with the national tendency of integrating the universities to the communities they belong. Further on, the objective was to transform the research into an industrial product that could eventually be produced and be an alternative in the market with computers that at the moment were imported. With this objective, the technology used for the development was TTL 7400 which was considered as the elements with greater probability of being produced in Argentina in the following years.

Figure 1 shows the Mini in Bikini on display at the Electrical Engineering and Computers Department.

(a) Front console (b) Cabinet

Fig. 1: Mini in Bikini: Cabinet with keys and the internal cards

3.1 General Architecture, Eng. Jorge Santos

The processor was designed using a classic Von Neumman approach. The architecture had nine registers of one byte. It could handle up to 64KB of primary memory and 16 peripherals. There were two types of instruction operands: short (1 byte) and long (2 bytes). Even if the general organization was based on 8 bits, each memory access read 16 bits. The following registers were defined: **Accumulator (A):** It had sixteen bits numbered from 0 to 15; **T:** this register had only one bit and was used together with **A** as a sign bit and to detect overflows; textbfC: this was an address register used to control the access to the main memory (this register had its own adder to compute the next instruction address) and **P:** this was the instruction register in which the instruction obtained from memory through **C** was copied for decoding. Bits 15-12 were used for the operation code, bits 11-10 were used to discriminate the memory page (0, 1, 2, 3); bit

9 was used as indirection bit and bit 8 the operand bit, while bits 7-0 were used for the address. The indirect addressing was used in the following way. In the address bits there was the memory address in which the address of the operand was found. The operand was then moved into an auxiliary register **D**.

The arithmetic and logic unit operated with the accumulator (**A**) and the second operand was the memory output, **(SO)**. Additionally, the register **A** could be incremented or decremented, while **SO** could only be incremented.

There were also some Input/Output peripherals to interact with the computer. The information flow within the processor was performed using a data channel that was arbitrated by the corresponding gates following a Lagrangian tree structure [5]. There were two memories, the RAM for reading and writing and the microprogramming memory only for reading. Figure 2 presents the graph representation of the processor registers, memory, keys and basic operations.

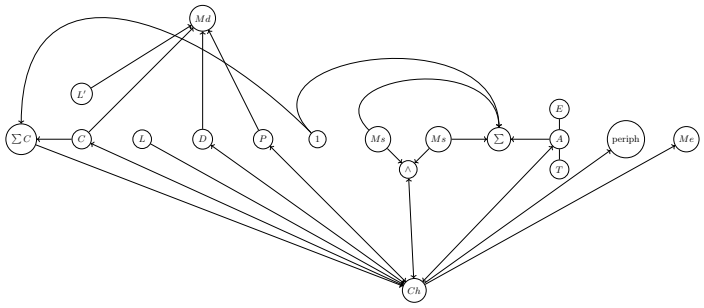

Fig. 2: Graph representing the Langragian tree

The elements in the graph are: $\sum C$: adder for register C; C: control address register; L': keys for address selection; L: keys for data; D: auxiliary register for instruction register P; Md: Memory input address; 1: one; Ms: Memory output register; $\sum$: General adder; A: Accumulator; E: Accumulator extension; T: Transport register; $\wedge$: And; Me: Memory input register; periph: Peripherals.

There were several sets of keys in the computer console that allowed the loading of registers and instructions. The Mini in Bikini console had sixteen keys for addresses and another sixteen for data. These keys were used to load the program on the computer. The arrow keys also functioned as a memory output register. Each register presented the output through small lamps that indicated the value of each bit.

The processor operated on a simple automata based on six phases implemented with a train of pulses. The last phase was larger in some cases, as to allow the propagation of the carry signal in the main adder, or shorter in others as to prevent delays in the execution of simple data transfers between registers or shift operations. The instruction cycle (at that moment it was called

[5] http://people.math.sfu.ca/ kyeats/teaching/math343/7-343.pdf

"*compass*") had the following phases: (0) Instruction fetch; (1) Read instruction; (2) Operand address fetch (with indirect addressing mode); (3) Load operand address; (4) Operand fetch; (5) Load operand and execute operation (instruction). There were sixteen instructions and one of them was expanded to another sixteen microinstructions completing the instruction set. In Tables 1 and 2 the instruction set and microinstructions are presented.

Table 1
Instruction Set: Macroinstructions

Group	Nemonic	OC	Description	Spanish description
I	ca	0000	load accumulator	cargar acumulador
I	ia	0001	AND accumulator	Y acumulador
II	aa	0010	ADD accumulator with memory	adicionar acumulador
II	ra	0011	SUBSTRAC accumulator	restar acumulador
II -III	sa	0100	JUMP for accumulator	saltar acumulador
I	sm	0101	JUMP for memory	saltar memoria
IV	ta	0110	TRANSFER accumulator	transferir acumulador
	ss	0111	JUMP to subroutine	saltar subrutina
I	si	1000	unconditional JUMP	salto incondicional
II	ma	1001	MULTIPLY accumulator	multiplicar acumulador
II	da	1010	DIVIDE accumulator	dividir acumulador
	mi	1011	Microinstructions	micro instrucciones
		1100	free	libre

Table 2
Instruction set: Microinstructions

Group	Nemonic	OC	Description	Spanish description
I	if	1011:0000	ghost instruction	instrucción fantasma
I	ka	1011:0001	COMPLEMENT accumulator	complementar acumulador
II	au	1011:0010	INCREMENT accumulator	aumentar acumulador
	ru	1011:0011	DECREMENT accumulator	restar acumulador
I	di	1011:0100	SHIFT accumulator left	desplazar izquierda
I	dd	1011:0101	SHIFT accumulator right	desplazar derecha
I	ri	1011:0110	ROTATE accumulator left	rotar izquierda
I	rd	1011:0111	ROTATE accumulator right	rotar derecha
I	la	1011:1000	CLEAR accumulator	limpiar acumulador
III	sb	1011:1001	JUMP for bit	saltar por bit
		1011:1010-1110	free	libre
I	pm	1011:1111	HALT processor	parar máquina

3.2 Arithmetic Unit, Eng. Lidia Luisoni

The logic gates used in the implementation of this unit were the following. For the adders SN 7480, Flip-Flops D dual SN 7474, SN 7400, SN 7401, SN 15946, SN 7410, MC 7453, MC 7460 and MC 7404. It implemented the following instructions: ca, ia, aa, ra, ka, au, ru, di, dd, ri, rd, la. The following registers were also implemented within this unit: A, E, and the bank for performing additions [20]. Multiplication and division instructions were implemented by software as the requirements to do this in hardware were not available at the moment in which the computer was designed. The operation codes were reserved for future improvements of the processor.

3.3 Control Unit, Eng. Néstor González

The control unit was based on a pulse generator and a decoder that together with the instruction decoders and a glue logic created a pulse train necessary to evolve the processor for the execution of each instruction. This pulse train incremented the **C** register, allowed the presentation of data and addresses, and opened the data channel for exchanges between registers, memory, and operations bank. Each pulse in the train was noted P_0, P_1, ..., P_9. [21]

The data channel was unique and it was used to move data from register to register, register to memory, memory to register, peripheral to accumulator and accumulator to peripheral and from the bank of operations to accumulator. In order to allow the loading of memory from the console, the data keys were used. The different accesses to the channel were managed by the control unit except for the transfer from the console to memory that was handled by an asynchronous pulse generated in the console that presented either data or instructions to be written into the memory.

Pulse train generator It was implemented with a programmable counter that was configured according to the instruction being executed. All instructions had in common the first two pulses for searching for instructions. They were: P_0 presented **C** as the memory address to fetch the instruction, and **C** was incremented after that; P_1 loaded **P** with the contents of the memory read.

After this, if it was a macroinstruction, the next pulse the operands were fetched. This could be done using a direct or indirect addressing. In the latter case the next two pulses implemented the following operations: in P_2 the content of byte 0 of **P** together with the page index were used to access the memory; in P_3 byte 0 of **P** was copied to concatenate with **C** the memory address obtained in the previous pulse. After these two pulses the next one was used as in the case of direct addressing: in P_4 the operand address is presented and copied it to the memory output register Ms and **C** is incremented.

The pulses used the two phases in the following way. During the high level phase, the channel transfer was enabled while in the low level phase the data was actually transferred.

The microinstructions did not use external operands. In these cases the pulses P_3 to P_5 were skipped. The pulse train generator was built using a binary counter from 0 to 9 designed using the Veitch-Phister method [22]. The counter could be programmed by forcing the flip-flops states using the clear and reset inputs of the flip-flop D.

Since the microinstructions had the two more significant bits equal to 1, they were easily decoded so the counter could be programmed to skip the unnecessary pulses. In the case of macroinstructions, when the direct addressing was used, pulses P_2 and P_3 were skipped. Like in the previous case a combinatorial circuit was used to program the involved flip-flops.

There were four group of instructions. In group I the instructions used up to P_5 were they finished and thus the counter had to return to zero to begin a new cycle. For this all the instructions in this group forced the transition. In

group II the counter ran up to state 9 and returned automatically to 0. For these instructions it was necessary to generate a wide pulse that could hold between P_5 and P_9. In the case of instructions in group III, the pulses P_5 and P_6 were skipped. In group IV the instructions used all the pulses.

The pulses were identified using decoders and to provide stability in the transitions, the flip-flops changed state with the complement of the clock.

Decoders and Instructions The processor had 23 instructions, 9 of them interacted with the memory, only 3 interacted with peripherals and the rest were microinstructions. The operation code was defined by the 4 most significant bits. From the 16 possibilities, 9 were used as macroinstructions, 3 were used for peripherals which were identified by the following 4 bits (16 in total), and when the code was 1100, the next four bits were used to defined the microinstructions. Multiplication and division were not implemented. In the case of microinstructions, 5 possibilities were reserve for future improvements. After the operation codes, the following three bits were used to identify the kind of addressing and the second byte for the address. The decode logic was implemented using four input gates and where used together with the flip-flops to obtain all the possible combinations for the operation of the processor.

Command logic A set of combinatorial logic circuits were designed to command the following operations: data transfer, increment of register **C**, reading and writing of memory, address presentation and handling of the arithmetic unit. In order to perform a transfer, the channel was yielded to the information that it had to be copied while a clock pulse was provided to the flip-flops on which the data had to be registered. In [21] the circuit schematics can be found. Together with this, the control unit activated the bank of operations for shift and rotation operations and to generate the interrupt signals.

Program counter The register **C** had different kinds of increments according to the executing instruction. In some cases it incremented in one unit and in others in two. For this the best solution was to use four MC7483 (full four bit fast adder with carry) to facilitate the operation of this register.

Memory address presentation There were four different sources. 1) Peripherals, 2) Register **C**, 3) Byte 0 of **P** concatenated with **D**, 4) Console keys. In the first case, the peripheral presented an address (identified with the peripheral) in which the processor read a branch instruction. The second case corresponded to the normal operation of the processor in which register **C** was incremented to read the next instruction. The third case was used by instructions that need the read/write operands/results from/to memory. For this, they used the register **P** concatenated with register **D**. The fourth case corresponded to the load of memory through the use of the keys in the console.

Channel Implementation The channel was implemented using AND-OR MC7453 gates. All these were connected to a MC7430 NAND gate that determined the channel.

Overflow detection When the accumulator sign bit was different from the transport bit, the overflow condition was obtained and reported to validate the result of the operation. This happened with arithmetic operations, addition and subtraction, and logical displacement operations. Detection was performed with combinatorial logic that stopped the processor from executing and reset its instruction register.

3.4 Interface Unit with Interrupt Capability, Eng. Ricardo Barrios

There was an important speed difference between the processor unit and the input/output peripherals that imposed the need to implement an interrupt driven unit. As there were several peripherals, the interrupts had different priorities. The interrupt system allowed a higher priority interruption while serving a lower one. Registers **C** and **A** were preserved while serving an interrupt, this was performed by programming. The latency associated to the interrupt service was at most the time needed to complete the longest instruction [23]. Each peripheral had a control card and its position determined the priority of the interrupt associated to that device. In this way a daisy-chain interrupt handling method was designed. There were only three instructions associated to the peripherals: `ap`, `te` and `ts`. These instructions were decoded in bits 15-12 and the next four bits identified one of the sixteen peripherals.

Control cards Each peripheral device had its own control card but all of them had flip-flop C for control and a flip-flop IP to mark a pending interrupt. Besides these two elements, the card had all the necessary control electronic circuits for the device.

At the moment of the implementation of the computer, only two devices were available: a Ferranti tape reader (300 characters per second) and a tape bunch Greed (30 characters per second). Unfortunately, none of these devices were found at the Department of Electrical Engineering and Computers for exhibition. The Mini in Bikini prototype is being exposed in the entrance of the Digital Systems Laboratory but none of the peripherals have survived.

Interrupt system In the last pulse of the instruction the interrupts were checked. As there were instructions that finish in P_5 and others in P_9, these were pulses in which the control unit revised the interrupt requests. During the last pulse of the instructions, the unit control checked the flip-flops associated to the interrupts and copying their states to another set of flip-flops. The output of these flip-flops were connected to a NAND that produced the Interrupt signal for the processor. With this signal the Control Unit stopped the program execution

and served the interruption in the next cycles. The interrupt priority system was based on a daisy chain so the proximity of the interrupt source to the processor determined the priority.

Once the interrupt was recognized, the processor executed the routine associated to the peripheral. For this, the address to jump in memory was hardwired in the same way it was the register **C**. Each device had a unique address so it was possible to enable at the time of the interrupt acknowledgment the access to the memory. In order to guarantee the correct priority order in the execution of nested interruptions, a third line of flip-flops name Blocking flip-flops was incorporated. For more details on the implementation of the interrupt system [21] can be read.

In case the last instruction of the program was to stop the processor (`pm`), the system continued working until the peripherals had finished their execution. For this a special logic circuit was included to avoid the shut down while there was a pending printing process.

Pulse and cycle instruction generation In order to debug the operation of the computer and to watch the evolution of the different registers there was an option to run the processor in a step by step operation including the possibility of executing a one pulse step or a whole machine cycle. For this, the console had three keys that defined the continuous or discontinuous operation, another one that defined if the execution was performed by instruction cycle or pulse and the last one was the start pulse to begin the execution. There was a fourth key that resets the computer when a program was finished, with this key several flip-flops were set to initial values.

Clock implementation The clock was implemented using two mono-stables and a NAND gate. The period was set to 320ns with a high state of 150ns. The circuit was evaluated under extreme conditions of temperature to check for its stability.

3.5 Memory implementation and improvements

After the development of the Mini in Bikini, other students worked on the computer extending and improving its operation. The student Ánibal Gil designed and installed a bipolar memory of four registers of 16 bits each one. The memory was designed using flip-flops D that operated synchronously. At the moment of connecting the new element to the computer the operation of the keys was reconfigured and some microinstructions were modified. While implementing, some propagation hazards were found in the pulses train that were resolved by introducing delay lines with mono-stables and inverters [24].

After this memory development, Eng. Rodolfo del Castillo did his Final Project designing a RAM memory based on modules MOS modules. The memory chips worked with 5V source voltage and could be ordered in 2K words of 16 bits each or 4K bytes. The project considered the possibility of expanding

the memory introducing new cards up to 32K words of 16 bits or 64K bytes. The memory has a bit parity redundancy every 8 bits detecting 100% of one bit error, 75% of two bits and for more bits error it tends to 50% asymptotically. The access time was 1 μs.

The memory was built using MOS cell units organized in what was called Memory Array. To access each cell, there is a decoder and an enable signal (H_0, H_1). The necessary information for to operate the memory was stored in the following registers: Address register (RD): 16 bits; Input register (RE_0, RE_1): for the low and high parts of the memory word (8 bits each); Control register (RC): it had only one bit, it could be 1 for writing and 0 for reading and to access 8 or 16 bits; Error register (RDE): it had only one bit and indicated if the memory was operating without errors. The following logic circuits were designed and implemented: Input selector (SE): it has 8 selectors with 2 inputs; Output selector (SS): it has 8 selectors with 2 inputs; Input parity detector (DPE): one for each memory byte; Output parity detector (DPS): one for each memory byte; Memory control (MC): it is a circuit that for each memory enable signal produced the necessary pulses for each register, chosed the appropriate input for each selector and enabled the correct memory arrays with the signals H_0 and H_1; Error detector (DE): it is the circuit in charged of checking the odd parity in the output.

The memory was implemented and proved with the Mini in Bikini computer. For further details on its implementation and tests the reader can check the original manuscript in [25].

4 Mini in Bikini Emulator

Prof. del Castillo developed a java-script emulator for the Mini in Bikini computer [6]. The emulator presents the Mini console with its keys and lights and it can be programmed exactly in the same way as it was the original one. Following the process by switching the different keys the program may be loaded into the memory and executed.

Prof. del Castillo has incorporated new opportunities to the Mini by adapting a compiler in such a way that using the GNU Assembler directives a program can be written using the Mini Assembler and it can be compiled to a binary code. The emulator provides the possibility of using and adaptation of the input/output unit developed by Barrios and the memory developed by del Castillo himself. With it the memory can be loaded as if it was read from the tape reader and the output written into an ASCII text file as if it was punched in cards.

The compiler produces two files: the binary one (`hex`) that is loaded into the memory and the `lst` one that shows for each memory address used, the binary codes of the instructions, variable values, the assembler nemonics, labels and directives. Using the keys in the console, the memory contents can be compared with the `lst` file for verification.

[6] https://rdc.fi.uncoma.edu.ar

The emulator uses an actual picture of the Mini console. Each key can be switched and the leds will turn on when there is a logical one in that bit. When pulsed the reset switch the memory of the Mini is cleared as well as the registers. Just like in the original prototype, the emulator user should follow the steps necessary to load a program in memory and execute it.

With the emulator, Prof. del Castillo has proved the Mini in Bikini was indeed a general purpose stored-program computer. With just twenty-three instructions, the Mini may execute any program. During its life, the Mini in Bikini was used to teach computer hardware architectures so programs were short to show the specific behavior of the different parts. The emulator simulates the Mini in Bikini in all its characteristics, so the execution of the programs can be performed by instruction cycle (if the selection key is set for that) or state by state. In fact, the actual procedures to load the program and data in the emulator are exactly the same as those performed in the Mini in Bikini. In the future more complex programs may be prepared and the behavior of the computer can be further explored and even compared to other machines of the time.

5 Final remarks and conclusions

The computer was built in the Digital Systems Laboratory by a team of three students (Luisoni, Barrios and González) under the supervision of Prof. Santos. Later the memory unit was developed in two stages first using simple Flip-Flops D (Gil) and later using MOS circuits (del Castillo). It used simple gate logic available at the moment in Argentina and provided a simple but still powerful set of 23 instructions. At the moment of its conception the Mini in Bikini had research interest as the concept was being impulsed by computer manufacturers. However, In the early years of the 70s, INTEL successively brought to the market the first 4-bit microprocessor, the 4004 (1971), the first 8-bit one, 8008 (1972) and the second, which would mark the beginning of a new stage, the 8080 (1974). One year later, in 1975 Motorola produced the 6800 and a long race started between the giants. Personal computers finally prevailed, displacing mini computers from the market. From 1974 till 1980, the Mini was used in the Lab to teach computer architecture. Even if the advent of modern microprocessors turned quickly the Mini concepts obsolete it should be considered the design and implementation of the Mini in Bikini a landmark in the computer evolution history within Universidad Nacional del Sur and Argentina.

The military coup in 1966 caused the resignation of a large proportion of professors at Universidad de Buenos Aires but that was not the case at Universidad Nacional del Sur. This fact allowed the continuity of some of the research groups and is one of the causes for which the Mini in Bikini project was developed. In the following ten years there was great instability at UNS with changes in the academic organization, layoffs and reinstatements, and student conflicts among many others [26–28]. That process ended with the military coup in 1976 and the massive layoffs of teachers (professors and teaching assistants). In 1983 with the return of democracy, after a short normalization period, the national universities

autonomy was recovered allowing a slow recovery of the full academic life that continues until today.

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