Una aproximación histórica al desarrollo de una minicomputadora en la Universidad Nacional del Sur: la Mini en Bikini
Lucía Bracamonte , Rodolfo del Castillo, Rodrigo Santos
SADIO Electronic Journal of Informatics and Operations Research (EJS) Vol. 24 No. 2 (2025) e-ISSN 1514-6774
https://doi.org/10.24215/15146774e085 | https://revistas.unlp.edu.ar/ejs
Sociedad Argentina de Informática e Investigación Operativa | Universidad Nacional de La Plata | Buenos Aires | Argentina

Una aproximación histórica al desarrollo de una minicomputaodra en la Universidad Nacional del Sur: la Mini en Bikini*

Lucía Bracamonte[1], Rodolfo del Castillo[2], Rodrigo Santos[3]

[1] Centro de Estudios Regionales "Prof. Félix Weinberg",
Universidad Nacional del Sur, CONICET, Bahía Blanca, Argentina,
luciab@criba.edu.ar
[2] Dep. Ing. de Computadoras, Facultad de Informática,
Universidad Nacional del Comahue, Argentina
rolo@uncoma.edu.ar
[3] Dep. Ing. Eléctrica y de Computadoras, Instituo de Ciencias e Ingeniería en Computación,
Universidad Nacional del Sur - CONICET, Bahía Blanca, Argentina,
ierms@uns.edu.ar

Abstract. A mediados de los años sesenta, varias empresas construyeron minicomputadoras que se utilizaron en la industria y la administración. Sus principales características eran su tamaño y bajo costo. Naturalmente, su potencia de procesamiento no era tan grande como la de las mainframes, pero podían brindar servicios a empresas medianas y pequeñas. La posibilidad de desarrollar una industria nacional de fabricación de computadoras era una idea compartida por muchas personas en Argentina, provenientes del ámbito académico, militar, privado y gubernamental. El profesor Jorge Santos, entusiasmado con esta idea, promovió el diseño e implementación de una minicomputadora por parte de un grupo de estudiantes a principios de los años setenta. El nombre de la computadora era "Mini en Bikini". Se presenta una breve reseña del contexto político y económico, junto con el desarrollo de la ingeniería y la ciencia informática en el momento de la concepción del proyecto. Se presentan los detalles técnicos de esta minicomputadora, junto con un emulador desarrollado por el profesor del Castillo muchos años después.

Keywords: Historia de computación · Mini Computadoras · Computadoras universitarias · Educación con computers.

* Este trabajo se hizo con financiamiento de la Universidad Nacional del Sur.

Received May 2025; Accepted June 2025; Published July 2025

A history approach to the development of a minicomputer in Universidad Nacional del Sur: the Mini in Bikini*

Lucía Bracamonte[1], Rodolfo del Castillo[2], Rodrigo Santos[3]

[1] Centro de Estudios Regionales "Prof. Félix Weinberg",
Universidad Nacional del Sur, CONICET, Bahía Blanca, Argentina,
luciab@criba.edu.ar
[2] Dep. Ing. de Computadoras, Facultad de Informática,
Universidad del Comahue, Neuquén, Argentina
rolo@uncoma.edu.ar
[3] Dep. Ing. Eléctrica y de Computadoras, Instituo de Ciencias e Ingeniería en Computación,
Universidad Nacional del Sur - CONICET, Bahía Blanca, Argentina,
ierms@uns.edu.ar

Abstract. In the mid sixties, several companies built mini computers that were used in the industry and administration. The main characteristics of the minis were the size and low cost. Naturally, the computing power was not as large of those of the mainframes, but they could provide services in middle and small companies. The possibility of developing a national industry to build computers was an idea shared by many persons in Argentina from the academia, the military, the private sector and the governments. Prof. Jorge Santos was enthusiastic about this and promote the design and implementation of a mini computer by a group of students in the first years of the seventies. The name of the computer was "Mini in Bikini". A short review on the political and economic context is presented together with the computer engineering and science development at the moment of the project conception. The technical details of this mini computer are presented together with an emulator developed by Prof. del Castillo many years later.

Keywords: Computer history · Mini Computers · University computers · Education with computers.

1 Introduction

In this work we present the history of the Mini in Bikini, a University made mini computer developped by Prof. Santos and a group of students at Universidad Nacional del Sur. This paper extends a previous one presented at the "Simposio Argentino de Historia de la Tecnología y la Información" that took placed in the 53rd JAIIO in 2024, Bahía Blanca, Argentina [Castillo et al., 2024].

* This paper received financial support from Universidad Nacional del Sur

Mini computers were a solution developed by several computer manufacturers like Digital Equipment Corporation, Computer Automation to provide low cost computers that were small in size and did not require special electrical and cooling systems to operate. The success of this kind of computers was the generalization of the access to this technology for small companies and administrative offices. The minis come with an operating system, several input/output possibilities and many times the capability of increasing their computing power by putting them to work in a network.

The more successful period for the minis is from mid sixties to mid seventies. Even though the microprocessors are born in the early years of 1970, and the Personal Computer (PC) in the late years of that decade, it is not until the mid eighties that the PCs are in a position to replace commercially minicomputers.

In this paper we present a historical context of the Argentina in the period 1955-1976 and the way in which the computer science and engineering evolved. In particular we add to the previous version of this work and to differentiate it, a brief description of the fashion of the time in relation to the technological independence, a more detailed description of the memories implemented in the Mini and more details on the emulator developed by Prof. del Castillo.

Organization: The rest of the paper is organized in the following way. Section 2 presents the historical context in Argentina and describes the evolution of the computer science and engineering first years. In Section 4 the fashion of the time related to the technological independence movement is presented and the way in which this impulsed the development of the Mini in Bikini at UNS. In Section 5 the Mini is described in all its components. Section 6 presents the emulator and Section 7 provides the conclusions and future work.

2 Historical context in Argentina

Bahía Blanca is a city in the southwest of Buenos Aires province that hosts one of the most important harbours in the country. The deepwater commercial port for exporting grain, fuel, and fruit established the city as a development hub and a road and rail hub. For years, the port's commercial influence fueled the idea of establishing a new province with its capital in the city. The middle of the Twentieth Century, was a period of political effervescence and social mobilization in Argentina. Civilian and military governments alternated in power, but together with the business community, they maintained the idea of creating a hub of economic and cultural development in the city. The town became the center of an area of influence that brought together fifteen districts of the province of Buenos Aires with projection over the provinces of La Pampa, Río Negro and Neuquén. The number of inhabitants of the district went from 126,669 in 1960 to 182,158 in 1970 [Bracamonte and Cernadas, 2018]. Half of them were part of the middle income sectors with aspirations for social advancement through education, in particular by following a university career.

After the fall of President Juan Domingo Perón in 1955, higher education institutions were intervened. In Bahía Blanca, the Instituto Tecnológico del Sur

became a decentralized entity until it was granted the university status. The new interventor, with support from various social sectors, decided to pressure the government through a strike. As a consequence, by means of decree-law No. 154, the Universidad Nacional del Sur (UNS) was created.

With the Peronist party outlawed, Arturo Frondizi emerged victorious in the 1958 elections. He proposed a developmental agenda aimed at transforming the nation, which included the establishment of institutions for higher education focusing on technical training that were not in the orbit of the State. This initiative sparked a debate known as "secular or free", concerning the equality of state and private universities in vocational training and whether the former held superiority, a discussion that also involved the UNS. In 1962, Frondizi was overthrown by a new military coup, whose political repercussions were echoed in Bahía Blanca's university community. One year later, again with the Peronism banned, Arturo Illia was elected President. Throughout those years, despite the turbulent national backdrop, the fragmentation of the student movement, labor disputes among non-teaching staff, and challenges related to funding and infrastructure, the UNS had established itself by expanding its academic connections and enhancing its regional presence, while also benefiting from significant grants [Orbe, 2006].

In 1966, amid the declining authority of the national government and the potential resurgence of Peronism or the rise of leftist revolutionary movements, a military coup led by Juan Carlos Onganía ousted the president. This shift marked a transition from republicanism to corporatism, with a repressive model put in place that impacted trade unions, political parties, and student movements. The first armed organizations were born as a consequence of the political radicalization of youth groups. Universities were one more time intervened and the academic autonomy was put to an end with the objective of controlling the student movements and the political activities within the institutions. This implied the annulment of tripartite government and student participation in university politics. The majority of national universities rose up in open opposition to the government, leading to the resignations of authorities and professors. At the UNS, the rejection was manifested through statements by teachers, groups of graduates and students, and restrictive measures on political activity were quickly implemented. Student unrest was immediate, leading to increased surveillance, incidents, arrests, injuries, and raids targeting those suspected of being communists or subversives. Nevertheless, in terms of tangible developments, the UNS held promising prospects by the late sixties, thanks to land acquisitions, infrastructure improvements, and modernization efforts [Orbe, 2006].

Onganía held the presidency until 1970, when he was succeeded by General Roberto M. Levingston, who was later replaced by General Alejandro A. Lanusse in 1971. That year saw a surge in violence that directly impacted university communities. The escalating discontent compelled the military government to pursue an electoral solution, allowing for Perón's return to the country while prohibiting his candidacy. In 1973, elections were held, resulting in a victory for the formula led by Héctor Cámpora. As a new institutional phase began, several

professors and authorities at the UNS submitted their resignations. Shortly after, the president stepped down to initiate a new election, which ultimately led to Perón's win. In this environment, University Law No. 20,654 was enacted to facilitate the normalization of higher education institutions.

The president's death in 1974 led to a surge in violence, exacerbating an already critical economic and political crisis. The intensifying conflict between the most militant factions of both the left and right — Peronist and non-Peronist — significantly affected university life [Orbe, 2006]. Armed organizations became more active, prompting a harsh crackdown by the Armed Forces. Concurrently, paramilitary groups known as Triple A, established by José López Rega, resorted to kidnappings and murders of opponents, including university students affiliated with Marxist ideologies. Incidents of student arrests and the dismissal of faculty members escalated rapidly. In 1974, Jesús "el Negrito" García was kidnapped and murdered, and in 1975, engineering student David "Watu" Cilleruelo was killed in the hallways of the UNS by a member of the custody of the interventor Professor Remus Tetu.

After the death of President Peron his wife María Estela Martínez, the Vicepresident, assumed the presidency of the country. One year and a half later, in 1976, another military coup deposed her. The new regime called itself the "National Reorganization Process" promoted State terrorism and the violation of public and individual freedoms as the central axis of its management. In Bahía Blanca, the repressive climate was particularly intense as important military units from the Navy and the Army were hosted. This accentuated the terrorist action at the same time that the presence of the journalistic multimedia led by La Nueva Provincia legitimized the government's actions in the political and economic level [Cernadas and Marcilese, 2018]. A control and surveillance device was implemented in the universities over the administrative and teaching staff and also on the students, aimed at neutralizing the sectors classified as subversive, which generated a latent and effective threat of arrest, kidnapping, torture, disappearance or death. In addition, the operation of student centers was prohibited, disciplinary regulations were tightened, study plans were changed, programs and bibliography were censored, restrictions on entry into social science courses were established, and fees were introduced [Santos La Rosa, 2018].

The democratic restoration would only occur in 1983 and would lead to the beginning of normalization processes in Argentine universities, including the UNS. Since its creation until that date, it had established itself as the most important educational and cultural institution in the region of influence of Bahía Blanca [Orbe, 2006]. Furthermore, despite the difficulties that his institutional life had faced, it had integrated with the environment and its teachers had generated academic contacts with national and foreign peers.

2.1 Computer Science and Engineering first years

Beginning in 1956, Universidad de Buenos Aires (UBA) embarked on a significant modernization effort, with the School of Exact and Natural Sciences (FCEN) at its forefront. In this setting, late in 1957, the FCEN council, led by

Dean Rolando Garcia, made the decision to establish an institute for computing studies called the "Instituto de Cálculo" (IC) and sought funding for a computer. To pursue this initiative, a three-member committee was formed, which included Manuel Sadosky, whose influence shaped the entire process. By 1958, after securing financial support from the newly established Consejo Nacional de Investigaciones Científicas y Técnicas (CONICET), a tender was issued for the acquisition of a computer. This led to the purchase of a Ferranti Mercury machine, which arrived in Buenos Aires in November 1960 and was fully operational by May of the following year, marking the beginning of academic computing in the country. Shortly thereafter, in 1963, the first undergraduate program related to computer science was introduced at the same faculty. During that period, computers were enormous and required specialized cabinets for housing, making their use relatively uncommon and akin to a rare luxury [Jacovskis, 2011] [4].

Simultaneously, at Universidad Nacional del Sur, a group of researchers initially engaged in a "Seminario de Computadoras" and later worked on a project to develop a national electronic computer called CEUNS [Carnota and Rodríguez, 2010], under the guidance of Prof. Jorge Santos. The two groups maintained a close relationship and collaborated extensively. Notably, the machine language for CEUNS was developed by Prof. Victoria Bajar, who had been working with Prof. Sadosky at UBA. Although CEUNS was ultimately not constructed, the project yielded several published findings in contemporary journals and conferences [Santos and Arango, 1957, Arango et al., 1966, Arango et al., 1968, Santos and Arango, 1970]. This initiative was crucial for the advancement and establishment of the computer engineering research group and served as a significant precursor to the Mini in Bikini project, which also took place under Prof. Jorge Santos's supervision ten years later, from 1973 to 1975. In 1978, a student further enhanced the computer by adding larger MOS memory modules.

The military coup in 1966 led by General Onganía was severely damaging to scientific progress in Argentina, particularly in emerging fields that had yet to be developed in the country. Many professors resigned from their posts and fled to countries such as Uruguay, Venezuela, Brazil, France, the United States, and the United Kingdom in protest against the suspension of university autonomy. This mass exodus resulted in the dismantling of research groups, primarily at the Universidad de Buenos Aires. In contrast, at Universidad Nacional del Sur, research groups continued their work because Rector Aziz Ur Rahman chose to remain in office under the dictatorial regime. As noted by Patricia Orbe: "Supported by a segment of the local university community, Dr. Rahman managed the affairs of UNS alongside Department Directors who were accountable to the National Executive Branch. There were some resignations from faculty members in protest against the new situation, but the intervention at the University in Bahía Blanca was not as extensive as it was in other higher education institutions" ([Orbe, 2006], pag. 132)[5]. Nonetheless, the student movement actively protested the military coup, advocating for university autonomy and co-governance. In mid-1967,

[4] Thanks to Prof. Raúl Carnota for the historical context at UBA.
[5] The authors translate the reference to English.

Rahman resigned, claiming he had fulfilled his mandate to maintain order, and was succeeded by Manuel Eduardo Gómez Vara as the interim appointee from the dictatorship.

While in 1966 the professors resigned in 1976 they were fired. The impact was extremely hard and needed a long time to recover. For example, it was not until the return of democracy that universities were in conditions to create Computer Science academic departments, at Universidad de Buenos Aires in 1985 [UBA, 2024] and at Universidad Nacional del Sur in 1994 [DCIC, 2024].

3 A short review on the evolution of computers

In 1948, the University of Manchester operated the first stored-program electronic computer, which was designed and developed by Frederic C. Williams, Tom Kilburn, and Geoff Tootill. Initially, the computer was created to demonstrate the efficacy of Williams's tube memory, but it ultimately confirmed the feasibility of a general-purpose stored-program computer. The first program executed on this machine was written by Alan Turing to calculate the highest proper divisor of 2^{18} by testing each integer from 2^{18} downward. The computation took approximately 52 minutes to complete. The machine had only seven instructions and was referred to as the Manchester Baby [Manchester, 2024b]. This computer would later evolve into the Ferranti Mark I, which became the first commercial general-purpose computer [Manchester, 2024a].

The IBM System/360 mainframe computer was introduced in 1964. With it, IBM purpose was to provide software stability in such a way that it did not has to be replaced when the hardware was updated. In this way, software and hardware were separated for the first time. The System/360 was used both for academic and commercial activities [IBM, 2024]. Companies could buy a small system and later enlarge it without having to change the software. It became a kind of standard de facto the pushed the creation of computer carreers around the world.

Although the concept of the System/360 change the concept of mainframes, they still represent a large investment for medium or small companies. The mini computers were thought to facilitate the incorporation of the computer to acadmic and commercial activities but without the requirements of the mainframes. In [Lazowska, 2024] there is a timeline with the evolution of mini computers and the concept definition. It is stated: "*It is intended for a single user or small group of users, it is physically small (at least compared to a mainframe system), and sells for a fraction of the price of a mainframe (often at least an order of magnitude less).*"

Up to the arrival of mini computers, a computer was a large machine deployed at a special place with several terminals. Its use was sophisticated and only a small number of persons were in conditions to program and use them. Opening the door of this technology to general "public" was in the mind of companies and scientists, specially to support automation in the industrial processes. At the time, the "mini" concept exist in fashion and cars, mini skirts, mini Cooper;

thus having a mini computer appeared as a possibility. The first ones were DEC PDP-1 and the CDC 160-A but it was not until 1970 that the term mini computer was used with the PDP-8/e. Mini computers evolved as new requirements were demanded until eventually this kind of computers weighted hundreds of kilograms and drew considerable power. In this scenario super mini computers were introduced.

Many companies were in the race to build minicomputers, among them Computer Automation produced a series that started with PDC 804 and PDC 804. PDC means Programmed Digital Controllers. The last one was introduced in 1969, built on diode-transistor logic (DTL) gates, it has 4KB of memory that can be extended upt to 16 KB. Two years later, this company introduced the Alpha 8 and Alpha 16 for processors of 8 and 16 bits respectively, based on DTL and transistor-transistor logic (TTL) components. The memory options were 4KB and 8KB and in some cases came with 16 KB magnetic core full cards. The input interface had a variety of options like a paper tape through a special board called the utility controller that was able to drive other peripherals like printers. There was a magnetic tape controller too. The programmer console had a row of toggle switches for data entry and boostrap routines [Computer, 2024]. Computer Automation named the Alpha 16 as Naked Mini when it was provided without the input/output interfaces and the power source. In the flyer of the computer they stated [Computer, 2024]:"*we had some simple, yet very ambitious goals. We wanted to offer a minicomputer that is -above all -easy to use. Even more, it has to be dependable and very low in cost. With no sacrifice in computer power.*"

Although Argentina was in the middle of a political and economic crisis, at Universidad Nacional del Sur the incentive to be part of the developing technology that would finally change the way in which we live today was intact. It was in this context that Prof. Jorge Santos led a group of students in the design and implementation of a mini computer to be used within the laboratory as a prototype and to be developed as a national computer in order to replace what at that moment was imported. The result was the Mini in Bikini, supposedly a bit better than the mentioned Naked Mini. The Mini in Bikini project was oriented to the teaching of processor architectures and its hardware operation but also a proof of concept that it was possible to build a low cost mini computer. Software was complimentary and just simple programs were prepared.

4 Preparing the land for the argentine minicomputer

Many of the people involved in the first computing activities in Argentina were working in the private sector in the beginning of the 1970s. For example, Sadosky and other former members of the 'Ìnstituto de Cálculo" founded the first consulting firm in the country dedicated to the development of computer-based software and mathematical models. The team that has worked at the Engineering School of Universidad de Buenos Aires in the development of "Computadora Electrónica de la Facultad de Ingeniería de Buenos Aires" CEFIBA, was reunited

in the Electronics Division of FATE, led by Roberto Zubieta. By 1971, FATE Electrónica had launched its first electronic calculators on the Argentine market and was planning the development of a minicomputer (Zubieta, 2009). Several others were still working at universities, large companies and some government agencies. At the UNS, as noted, activity in Digital Systems had not been interrupted, and other research centers existed in institutions such as the Scientific and Technical Research Institute of the Armed Forces (CITEFA) among others.

At the beginning of the seventies, it was already clear that technology and specially computers were going to be fundamental for the development [Nora and Minc, 1980]. As the technological gap separating central economies from those in the *third world* would grow, the Rome-based International Bureau for Informatics (IBI), an entity linked to UNESCO and chaired by Argentine Fermín Bernasconi, began preaching to the latter countries, warning of the risks of worsening technological dependence and urging them to embrace (Information and Communication Techonlogies) ICTs. The IBI insisted that the ICTs were not just another advanced technique but a key to defining the future development of societies [Carnota and Vianna, 2019]. For this, the IBI insisted to developing countries to define National Information Technology policies and to create the necessary offices in the central government to provide support to it. One of its first initiatives was to promote the convening of a Conference of Latin American Authorities in Information Technology (CALAI), the first edition of which was held in Buenos Aires in 1970 [Carnota and Vianna, 2019].

In Argentina, like in other countries in Latin America, the lack of independence in so many different aspects like politics, economics, culture, and technology was an issue for a wide part of the society. The growing role of computing in economic and social development mobilized a broad sector of researchers and professionals in the search for ways to break technological dependence in this field. This fact coincided with the technical possibility of developing minicomputers in non-centralized countries, combined with the accumulation of capabilities already honed in computing development in previous years, particularly at UNS.

In the last days of the military government started in 1966, there was in agenda the creation of a national minicomputer industry. This was motorized by the Ministry of Defense, in particular within the Navy, that was working within CITEFA under the led of Lieutenant Commander H. Leibovich. Besides this initiative, the private company FATE was pursuing its own mini computer and at UNS, Prof. Santos. In May 1973, days before the constitutional government took office, the Ministry of Defense organized a "Roundtable on minicomputer" were all the actors participate and present their opinions on the possibility of producing an argentine minicomputer [Ministerio de Defensa, Dirección General de Investigación y Desarrollo,]. In his participation, Santos stated the need to articulate a multi institutional project to unify resources and efforts in a coordinate way. Other opinions were oriented to doing a previous study of the state of the art in the academia and the industry to determine the situation. Unfortunately, this last proposal was followed with an important cost that prevent

the use of that financial support in the actual development of the hardware and software [Santos La Rosa, 1973]. Five months later, Santos organized at UNS a new round-table, "Mesa Redonda de Política Nacional de Computación", in which the necessity of a National Policy of Computation was stated in the final document.

5 Mini in Bikini

The mini computer project was developed by three students: Lidia Luisoni, Ricardo Barrios and Néstor González. Each one was in charge of a part of the computer's architecture guided by Prof. Jorge Santos. Later Aníbal Gil added a small bipolar memory also under the supervision of Santos, and three years later, Rodolfo del Castillo added a larger MOS RAM memory to the computer making it fully operational under the supervision of Mg. Jorge Ardenghi and Eng. Enrrique Arroyo.

The general aim of the project was to provide a mini computer for its use within the industry, commerce and scientific research. This project was aligned to the conclusions of the round-table mentioned before. The objective was also aligned with the national tendency of integrating the universities to the communities they belong. Further on, the objective was to transform the research into an industrial product that could eventually be produced and be an alternative in the market with computers that at the moment were imported. With this objective, the technology used for the development was TTL 7400 which was considered as the elements with greater probability of being produced in Argentina in the following years.

Figure 1 shows the Mini in Bikini on display at the Electrical Engineering and Computers Department.

(a) Front console (b) Cabinet

Fig. 1: Mini in Bikini: Cabinet with keys and the internal cards

5.1 General Architecture, Eng. Jorge Santos

The processor was designed using a classic Von Neumman approach. The architecture had nine registers of one byte. It could handle up to 64KB of primary memory and 16 peripherals. There were two types of instruction operands: short (1 byte) and long (2 bytes). Even if the general organization was based on 8 bits, each memory access read 16 bits. The following registers were defined:

- **Accumulator (A):** It had sixteen bits numbered from 0 to 15.
- **T:** this register had only one bit and was used together with **A** as a sign bit and to detect overflows.
- **E:** This was the extension register, it had sixteen bits and was used as an auxiliary register of **A** during mathematical operations.
- **C:** this was an address register used to control the access to the main memory. This register had its own adder to compute the next instruction address.
- **P:** this was the instruction register in which the instruction obtained from memory through **C** was copied for decoding. Bits 15-12 were used for the operation code, bits 11-10 were used to discriminate the memory page (0, 1, 2, 3); bit 9 was used as indirection bit and bit 8 the operand bit, while bits 7-0 were used for the address. The indirect addressing was used in the following way. In the address bits there was the memory address in which the address of the operand was found. The operand was then moved into an auxiliary register **D**.

The arithmetic and logic unit operated with the accumulator (**A**) and the second operand was the memory output, **(SO)**. Additionally, the register **A** could be incremented or decremented, while **SO** could only be incremented.

There were also some Input/Output peripherals to interact with the computer. The information flow within the processor was performed using a data channel that was arbitrated by the corresponding gates following a Lagrangian tree structure[6]. There were two memories, the RAM for reading and writing and the microprogramming memory only for reading. Figure 2 presents the graph representation of the processor registers, memory, keys and basic operations.

The elements in the graph are: $\sum C$: adder for register C; C: control address register; L': keys for address selection; L: keys for data; D: auxiliary register for instruction register P; Md: Memory input address; 1: one; Ms: Memory output register; $\sum$: General adder; A: Accumulator; E: Accumulator extension; T: Transport register; $\wedge$: And; Me: Memory input register; periph: Peripherals.

There were several sets of keys in the computer console that allowed the loading of registers and instructions. The Mini in Bikini console had sixteen keys for addresses and another sixteen for data. These keys were used to load the program on the computer. The arrow keys also functioned as a memory output register. Each register presented the output through small lamps that indicated the value of each bit.

[6] http://people.math.sfu.ca/ kyeats/teaching/math343/7-343.pdf.

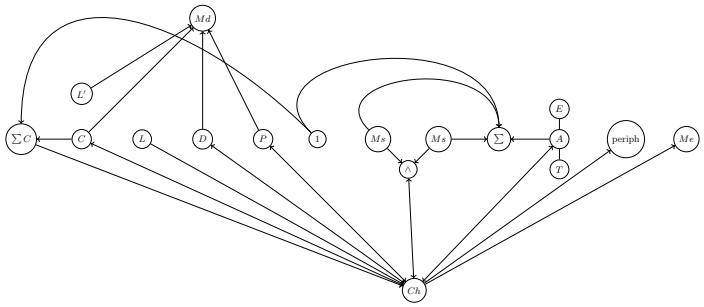

Fig. 2: Graph representing the Langragian tree

The processor operated on a simple automata based on six phases implemented with a train of pulses. The last phase was larger in some cases, as to allow the propagation of the carry signal in the main adder, or shorter in others as to prevent delays in the execution of simple data transfers between registers or shift operations. The instruction cycle (at that moment it was called "*compass*") had the following phases:

0. Instruction fetch.
1. Read instruction.
2. Operand address fetch (with indirect addressing mode).
3. Load operand address.
4. Operand fetch.
5. Load operand and execute operation (instruction).

There were sixteen instructions and one of them was expanded to another sixteen microinstructions completing the instruction set. In Tables 1 and 2 the instruction set and microinstructions are presented.

TABLE 1
Instruction Set: Macroinstructions

Group	Nemonic	OC	Description	Spanish description
I	`ca`	0000	load accumulator	cargar acumulador
I	`ia`	0001	AND accumulator	Y acumulador
II	`aa`	0010	ADD accumulator with memory	adicionar acumulador
II	`ra`	0011	SUBSTRAC accumulator	restar acumulador
II -III	`sa`	0100	JUMP for accumulator	saltar acumulador
I	`sm`	0101	JUMP for memory	saltar memoria
IV	`ta`	0110	TRANSFER accumulator	transferir acumulador
	`ss`	0111	JUMP to subroutine	saltar subrutina
I	`si`	1000	unconditional JUMP	salto incondicional
II	`ma`	1001	MULTIPLY accumulator	multiplicar acumulador
II	`da`	1010	DIVIDE accumulator	dividir acumulador
	`mi`	1011	Microinstructions	micro instrucciones
		1100	free	libre

5.2 Arithmetic Unit, Eng. Lidia Luisoni

The logic gates used in the implementation of this unit were the following. For the adders SN 7480, Flip-Flops D dual SN 7474, SN 7400, SN 7401, SN 15946,

TABLE 2
Instruction set: Microinstructions

Group	Nemonic	OC	Description	Spanish description
I	`if`	1011:0000	ghost instruction	instrucción fantasma
I	`ka`	1011:0001	COMPLEMENT accumulator	complementar acumulador
II	`au`	1011:0010	INCREMENT accumulator	aumentar acumulador
	`ru`	1011:0011	DECREMENT accumulator	restar acumulador
I	`di`	1011:0100	SHIFT accumulator left	desplazar izquierda
I	`dd`	1011:0101	SHIFT accumulator right	desplazar derecha
I	`ri`	1011:0110	ROTATE accumulator left	rotar izquierda
I	`rd`	1011:0111	ROTATE accumulator right	rotar derecha
I	`la`	1011:1000	CLEAR accumulator	limpiar acumulador
III	`sb`	1011:1001	JUMP for bit	saltar por bit
		1011:1010-1110	free	libre
I	`pm`	1011:1111	HALT processor	parar máquina

SN 7410, MC 7453, MC 7460 and MC 7404. It implemented the following instructions: ca, ia, aa, ra, ka, au, ru, di, dd, ri, rd, la. The following registers were also implemented within this unit: A, E, and the bank for performing additions [Luisoni, 1974]. Multiplication and division instructions were implemented by software as the requirements to do this in hardware were not available at the moment in which the computer was designed. The operation codes were reserved for future improvements of the processor.

5.3 Control Unit, Eng. Néstor González

The control unit was based on a pulse generator and a decoder that together with the instruction decoders and a glue logic created a pulse train necessary to evolve the processor for the execution of each instruction. This pulse train incremented the **C** register, allowed the presentation of data and addresses, and opened the data channel for exchanges between registers, memory, and operations bank. Each pulse in the train was noted P_0, P_1, ..., P_9. [González, 1974]

The data channel was unique and it was used to move data from register to register, register to memory, memory to register, peripheral to accumulator and accumulator to peripheral and from the bank of operations to accumulator. In order to allow the loading of memory from the console, the data keys were used. The different accesses to the channel were managed by the control unit except for the transfer from the console to memory that was handled by an asynchronous pulse generated in the console that presented either data or instructions to be written into the memory.

Pulse train generator It was implemented with a programmable counter that was configured according to the instruction being executed. All instructions had in common the first two pulses for searching for instructions. They were: P_0 presented **C** as the memory address to fetch the instruction, and **C** was incremented after that; P_1 loaded **P** with the contents of the memory read.

After this, if it was a macroinstruction, the next pulse the operands were fetched. This could be done using a direct or indirect addressing. In the latter case the next two pulses implemented the following operations: in P_2 the content

of byte 0 of **P** together with the page index were used to access the memory; in P_3 byte 0 of **P** was copied to concatenate with **C** the memory address obtained in the previous pulse. After these two pulses the next one was used as in the case of direct addressing: in P_4 the operand address is presented and copied it to the memory output register Ms and **C** is incremented.

The pulses used the two phases in the following way. During the high level phase, the channel transfer was enabled while in the low level phase the data was actually transferred.

The microinstructions did not use external operands. In these cases the pulses P_3 to P_5 were skipped. The pulse train generator was built using a binary counter from 0 to 9 designed using the Veitch-Phister method [Veitch, 1952]. The counter could be programmed by forcing the flip-flops states using the clear and reset inputs of the flip-flop D.

Since the microinstructions had the two more significant bits equal to 1, they were easily decoded so the counter could be programmed to skip the unnecessary pulses. In the case of macroinstructions, when the direct addressing was used, pulses P_2 and P_3 were skipped. Like in the previous case a combinatorial circuit was used to program the involved flip-flops.

There were four group of instructions. In group I the instructions used up to P_5 were they finished and thus the counter had to return to zero to begin a new cycle. For this all the instructions in this group forced the transition. In group II the counter ran up to state 9 and returned automatically to 0. For these instructions it was necessary to generate a wide pulse that could hold between P_5 and P_9. In the case of instructions in group III, the pulses P_5 and P_6 were skipped. In group IV the instructions used all the pulses.

The pulses were identified using decoders and to provide stability in the transitions, the flip-flops changed state with the complement of the clock.

Decoders and Instructions The processor had 23 instructions, 9 of them interacted with the memory, only 3 interacted with peripherals and the rest were microinstructions. The operation code was defined by the 4 most significant bits. From the 16 possibilities, 9 were used as macroinstructions, 3 were used for peripherals which were identified by the following 4 bits (16 in total), and when the code was 1100, the next four bits were used to defined the microinstructions. Multiplication and division were not implemented. In the case of microinstructions, 5 possibilities were reserve for future improvements. After the operation codes, the following three bits were used to identify the kind of addressing and the second byte for the address. The decode logic was implemented using four input gates and where used together with the flip-flops to obtain all the possible combinations for the operation of the processor.

Command logic A set of combinatorial logic circuits were designed to command the following operations: data transfer, increment of register **C**, reading and writing of memory, address presentation and handling of the arithmetic unit. In order to perform a transfer, the channel was yielded to the information that

it had to be copied while a clock pulse was provided to the flip-flops on which the data had to be registered. In [González, 1974] the circuit schematics can be found. Together with this, the control unit activated the bank of operations for shift and rotation operations and to generate the interrupt signals.

Program counter The register **C** had different kinds of increments according to the executing instruction. In some cases it incremented in one unit and in others in two. For this the best solution was to use four MC7483 (full four bit fast adder with carry) to facilitate the operation of this register.

Memory address presentation There were four different sources. 1) Peripherals, 2) Register **C**, 3) Byte 0 of **P** concatenated with **D**, 4) Console keys. In the first case, the peripheral presented an address (identified with the peripheral) in which the processor read a branch instruction. The second case corresponded to the normal operation of the processor in which register **C** was incremented to read the next instruction. The third case was used by instructions that need the read/write operands/results from/to memory. For this, they used the register **P** concatenated with register **D**. The fourth case corresponded to the load of memory through the use of the keys in the console.

Channel Implementation The channel was implemented using AND-OR MC7453 gates. All these were connected to a MC7430 NAND gate that determined the channel.

Overflow detection When the accumulator sign bit was different from the transport bit, the overflow condition was obtained and reported to validate the result of the operation. This happened with arithmetic operations, addition and subtraction, and logical displacement operations. Detection was performed with combinatorial logic that stopped the processor from executing and reset its instruction register.

5.4 Interface Unit with Interrupt Capability, Eng. Ricardo Barrios

There was an important speed difference between the processor unit and the input/output peripherals that imposed the need to implement an interrupt driven unit. As there were several peripherals, the interrupts had different priorities. The interrupt system allowed a higher priority interruption while serving a lower one. Registers **C** and **A** were preserved while serving an interrupt, this was performed by programming. The latency associated to the interrupt service was at most the time needed to complete the longest instruction [Barrios, 1974]. Each peripheral had a control card and its position determined the priority of the interrupt associated to that device. In this way a daisy-chain interrupt handling method was designed. There were only three instructions associated to the peripherals: `ap`, `te` and `ts`. These instructions were decoded in bits 15-12 and the next four bits identified one of the sixteen peripherals.

Control cards Each peripheral device had its own control card but all of them had flip-flop C for control and a flip-flop IP to mark a pending interrupt. Besides these two elements, the card had all the necessary control electronic circuits for the device.

At the moment of the implementation of the computer, only two devices were available: a Ferranti tape reader (300 characters per second) and a tape bunch Greed (30 characters per second). Unfortunately, none of these devices were found at the Department of Electrical Engineering and Computers for exhibition. The Mini in Bikini prototype is being exposed in the entrance of the Digital Systems Laboratory but none of the peripherals have survived.

Interrupt system In the last pulse of the instruction the interrupts were checked. As there were instructions that finish in P_5 and others in P_9, these were pulses in which the control unit revised the interrupt requests. During the last pulse of the instructions, the unit control checked the flip-flops associated to the interrupts and copying their states to another set of flip-flops. The output of these flip-flops were connected to a NAND that produced the Interrupt signal for the processor. With this signal the Control Unit stopped the program execution and served the interruption in the next cycles. The interrupt priority system was based on a daisy chain so the proximity of the interrupt source to the processor determined the priority.

Once the interrupt was recognized, the processor executed the routine associated to the peripheral. For this, the address to jump in memory was hardwired in the same way it was the register **C**. Each device had a unique address so it was possible to enable at the time of the interrupt acknowledgment the access to the memory. In order to guarantee the correct priority order in the execution of nested interruptions, a third line of flip-flops name Blocking flip-flops was incorporated. For more details on the implementation of the interrupt system [González, 1974] can be read.

In case the last instruction of the program was to stop the processor (`pm`), the system continued working until the peripherals had finished their execution. For this a special logic circuit was included to avoid the shut down while there was a pending printing process.

Pulse and cycle instruction generation In order to debug the operation of the computer and to watch the evolution of the different registers there was an option to run the processor in a step by step operation including the possibility of executing a one pulse step or a whole machine cycle. For this, the console had three keys that defined the continuous or discontinuous operation, another one that defined if the execution was performed by instruction cycle or pulse and the last one was the start pulse to begin the execution. There was a fourth key that resets the computer when a program was finished, with this key several flip-flops were set to initial values.

Clock implementation The clock was implemented using two mono-stables and a NAND gate. The period was set to 320ns with a high state of 150ns. The circuit was evaluated under extreme conditions of temperature to check for its stability.

5.5 Memory implementation and improvements. Eng. Aníbal Gil, Eng. Rodolfo del Castillo

The machine described in the previous section needed a memory to be programmed and became operable. Under the supervision of Santos, Aníbal Gil implemented a four 16 bit register bank memory based on bipolar technology in 1975 [Gil, 1975]. It was designed using flip-flops D operating synchronously. With this small memory it was possible to load very simple programs to demonstrate that the computer was working. At the moment of connecting the new element to the computer the operation of the keys was reconfigured and some microinstructions were modified. While implementing, some propagation hazards were found in the pulses train that were resolved by introducing delay lines with mono-stables and inverters.

With the memory implemented by Gil, the computer was used for teaching in basic computer architecture courses. Students learnt how to program in Assembler and they can verified the operation of the program by manually loading it into the Mini in Bikini and executing it step by step. In the projects reports there are several handwriting notes by Santos. One of them is an exercise he proposed for the laboratory exercises. *"Exercise #6: Lorenzetti (he was a teaching assistan)- With the instructions of the MiniB, write a program in assembler that move the contents of addresses 128 till 137 towards addresses 1024 till 1035."* In terms of Eng. Arroyo, with the memory the students can prepare short programs to perform simple arithmetic and logical operations[7].

The Mini in Bikini project contemplated the acquisition of MOS memory. Unfortunately, this was too expensive and out of the possibilities of the Digital Systems Lab at UNS. For this, Santos has applied for financial support at CONICET. The money arrived just after Santos was expelled from the University by the military intervention in June 1976. This forced the returned of the money and the project remained in stand by for the next two years.

In 1978, Eng. Rodolfo del Castillo did his Final Project designing a RAM memory based on MOS modules [del Castillo, 1978]. The memory chips worked with 5V source voltage and could be ordered in 2K words of 16 bits each or 4K bytes. The project considered the possibility of expanding the memory introducing new cards up to 32K words of 16 bits or 64K bytes. It also considered the possibility of being used for a new microprocessor platform that has been acquired by the laboratory, a PACE microprocessor from National. The memory has a bit parity redundancy every 8 bits detecting 100% of one bit error, 75% of two bits and for more bits error it tends to 50% asymptotically. The access time was 1 μs.

[7] Interview with Eng. Arroyo, January 2025.

The memory was built using MOS cell units organized in what was called Memory Array. To access each cell, there is a decoder and an enable signal (H_0, H_1). The necessary information for to operate the memory was stored in the following registers:

- Address register (RD): 16 bits
- Input register (RE_0, RE_1): for the low and high parts of the memory word (8 bits each).
- Control register (RC): it had only one bit, it could be 1 for writing and 0 for reading and to access 8 or 16 bits.
- Error register (RDE): it had only one bit and indicated if the memory was operating without errors.

The following logic circuits were designed and implemented:

- Input selector (SE): it has 8 selectors with 2 inputs.
- Output selector (SS): it has 8 selectors with 2 inputs.
- Input parity detector (DPE): one for each memory byte.
- Output parity detector (DPS): one for each memory byte.
- Memory control (MC): it is a circuit that for each memory enable signal produced the necessary pulses for each register, chosed the appropriate input for each selector and enabled the correct memory arrays with the signals H_0 and H_1.
- Error detector (DE): it is the circuit in charged of checking the odd parity in the output.

The memory was implemented and proved with the Mini in Bikini computer. For further details on its implementation and tests the reader can check the original manuscript in [del Castillo, 1978]. With this memory the Mini was capable of executing larger programs like doing loops for successive arithmetic and logical operations. However, just a few months later, the first microprocessors platforms from Intel arrived to the UNS and the courses were centered on them leaving behind the Mini in Bikini.

6 Mini in Bikini Emulator

Even if the Mini in Bikini was capable of executing programs of any kind, these should be written in Assembler and loaded into the memory instruction per instruction following a complex sequence with the front keys. Among the missing developments we can mention input/output devices for reading programs and writing results in an automatic way, a compiler and an operating system among others. These things were limitations that restricted the Mini's operability. Thirty years later, just before the pandemic Covid-19, Prof. del Castillo recovered the reports about the Mini in Bikini and developed a java-script emulator for the Mini in Bikini computer [8]. The emulator presents the Mini console

[8] https://rdc.fi.uncoma.edu.ar

with its keys and lights and it can be programmed exactly in the same way as it was the original one. Following the process by switching the different keys the program may be loaded into the memory and executed. In order to overcome the restrictions mentioned, Prof. del Castillo adapted the GNU Assembler compiler in such a way that a program developed with the Mini in Bikini Assembler can be compiled to a binary code. The emulator provides the possibility of using and adaptation of the input/output unit developed by Barrios and the memory developed by del Castillo himself. With it the memory can be loaded as if it was read from the tape reader and the output written into an ASCII text file as if it was punched in cards. In this way, the emulator developed by del Castillo provides the possibility of writing larger programs and to proving them.

The compiler produces two files: the binary one (`hex`) that is loaded into the memory and the `lst` one that shows for each memory address used, the binary codes of the instructions, variable values, the assembler nemonics, labels and directives. Using the keys in the console, the memory contents can be compared with the `lst` file for verification.

The emulator uses an actual picture of the Mini console. Each key can be switched and the leds will turn on when there is a logical one in that bit. When pulsed the reset switch the memory of the Mini is cleared as well as the registers. Just like in the original prototype, the emulator user should follow the steps necessary to load a program in memory and execute it.

With the emulator, Prof. del Castillo has proved the Mini in Bikini was indeed a general purpose stored-program computer. With just twenty-three instructions, the Mini may execute any program. During its life, the Mini in Bikini was used to teach computer hardware architectures so programs were short to show the specific behavior of the different parts. The emulator simulates the Mini in Bikini in all its characteristics, so the execution of the programs can be performed by instruction cycle (if the selection key is set for that) or state by state. In fact, the actual procedures to load the program and data in the emulator are exactly the same as those performed in the Mini in Bikini. In the future more complex programs may be prepared and the behavior of the computer can be further explored and even compared to other machines of the time. The emulator provides a third life to the Mini in Bikini project.

7 Final remarks and conclusions

The computer was built in the Digital Systems Laboratory by a team of three students (Luisoni, Barrios and González) under the supervision of Prof. Santos. A fouth student developed a reduced memory using simple Flip-Flops D (Gil) and three years later using MOS circuits (del Castillo) a larger one. It used simple gate logic available at the moment in Argentina and provided a simple but still powerful set of 23 instructions. At the moment of its conception the Mini in Bikini had research interest as the concept was being impulsed by computer manufacturers and there was a national interest in developing a computer national policy. However, in the early years of the 70s, INTEL successively brought

to the market the first 4-bit microprocessor, the 4004 (1971), the first 8-bit one, 8008 (1972) and the second, which would mark the beginning of a new stage, the 8080 (1974). One year later, in 1975 Motorola produced the 6800 and a long race started between the giants. Personal computers finally prevailed, displacing mini computers from the market in the mid 80s. From 1974 till 1979, the Mini was used in the Lab to teach computer architecture and assembler programming. Even if the advent of modern microprocessors turned quickly the Mini concepts obsolete it should be considered the design and implementation of the Mini in Bikini a landmark in the computer evolution history within Universidad Nacional del Sur and Argentina.

The Mini in Bikini was a project thought on two axes. As explained in Section 4, there was a fashion of time for the technological independence and an true opportunity to develop a national industry to design and build mini computers. The project as stated in the motivation sections of the reports written by Gonzalez, Luisoni, Barrios and Gil were oriented to obtain a prototype of this kind of computer that could be transferred to the private sector to develop a national computer. The other axe was related to the academics, research and teaching. The first axe was not possible as the military government economic policy destroyed in general the national industry privileging an open economy for which the country was not prepared. Besides this, the research group of Universidad Nacional del Sur was dismantled as the Professors were ejected from their positions (Santos, Pascual, Arango). With this situation, only the teaching axe remained until the advent of the microprocessor era.

The military coup in 1966 caused the resignation of a large proportion of professors at Universidad de Buenos Aires but that was not the case at Universidad Nacional del Sur. This fact allowed the continuity of some of the research groups and is one of the causes for which the Mini in Bikini project was developed. In the following ten years there was great instability at UNS with changes in the academic organization, layoffs and reinstatements, and student conflicts among many others [Bonavena, 2005, Califa, 2018, Romero et al., 2014]. That process ended with the military coup in 1976 and the massive layoffs of teachers (professors and teaching assistants). In 1983 with the return of democracy, after a short normalization period, the national universities autonomy was recovered allowing a slow recovery of the full academic life that continues until today.

References

Arango et al., 1966. Arango, H., Pascual, M., Valentinuzzi, M. E., and Santos, J. (1966). Threshold implementation of ternary systems. *IEEE Trans. Electron. Comput.*, 15(4):661–662.

Arango et al., 1968. Arango, H., Santos, J., and Chacur, A. (1968). Ternary cyclodecompositions. *IEEE Transactions on Computers*, 100(12):1175–1176.

Barrios, 1974. Barrios, R. (1974). Desarrollo de una Interfase con Capacidad de Interrupción. `https://rdc.fi.uncoma.edu.ar/docs/`. Accessed: 2024-03-09.

Bonavena, 2005. Bonavena, P. A. (2005). Notas sobre el movimiento estudiantil de Bahía Blanca (1966-1973). In *X Jornadas Interescuelas/Departamentos de Historia*.

Escuela de Historia de la Facultad de Humanidades y Artes, Universidad Nacional del Rosario. Departamento de Historia de la Facultad de Ciencias de la Educación, Universidad Nacional del Litoral.

Bracamonte and Cernadas, 2018. Bracamonte, L. and Cernadas, M. (2018). La sociedad bahiense: evolución poblacional, movimientos inmigratorios y formas de sociabilidad. In Cernadas, M. and Marcilese, J., editors, *Bahía Blanca siglo XX: historia política, económica y sociocultural*, pages 103–151. EDIUNS, Bahía Blanca.

Califa, 2018. Califa, J. S. (2018). La amenaza roja. la intervención a la uba durante 1966 vista desde el golpismo interno. *Contemporanea, Historia y problemas del siglo XX*, pages 35–49.

Carnota and Rodríguez, 2010. Carnota, R. and Rodríguez, R. (2010). Fulgor y ocaso de ceuns. una apuesta a la tecnología nacional en el sur de argentina. In *Anales del I Simposio de Historia de la Informática en América Latina y el Caribe, en el XXXVI CLEI*.

Carnota and Vianna, 2019. Carnota, R. and Vianna, M. (2019). En procura de autonomía tecnológica e integración regional. iniciativas de cooperación latinoamericana en informática (1970/1990). *Pasado abierto*, 5(10).

Castillo et al., 2024. Castillo, R. d., Bracamonte, L., and Santos, R. (2024). Mini in bikini: A ttl university made computer at universidad nacional del sur. In *Simposio Argentino de Historia, Tecnologías e Informática (SAHTI 2024)-JAIIO 53 (Universidad Nacional del Sur, 12 al 16 de agosto de 2024)*.

Cernadas and Marcilese, 2018. Cernadas, M. and Marcilese, J. (2018). El arduo camino de la democracia en Bahía Blanca: partidos, elecciones y activismo social. In Cernadas, M. and Marcilese, J., editors, *Bahía Blanca siglo XX: historia política, económica y sociocultural*, pages 37–102. EDIUNS, Bahía Blanca.

Computer, 2024. Computer, A. (2024). Naked mini/alpha 16. http://s3data.computerhistory.org/brochures/computerautomation.nakedmini-alpha16.1972.102646111.pdf. Accessed: 2024-03-09.

DCIC, 2024. DCIC (2024). Historia del Departamento de Ciencias e Ingeniería de Computación, Universidad Nacional del Sur. https://cs.uns.edu.ar/~devcs/institucional/historia. Accessed: 2024-03-09.

del Castillo, 1978. del Castillo, R. (1978). Memoria Semiconductores. ttps://rdc.fi.uncoma.edu.ar/docs/. Accessed: 2024-03-09.

Gil, 1975. Gil, A. (1975). Instalación de una memoria bipolar de 4x16 palabras y revisión crítica del procesador. https://rdc.fi.uncoma.edu.ar/docs/. Accessed: 2024-03-09.

González, 1974. González, N. (1974). Desarrollo de una Unidad de Control de una mini computadora. https://rdc.fi.uncoma.edu.ar/docs/. Accessed: 2024-03-09.

IBM, 2024. IBM (2024). Ibm 360. https://www.ibm.com/history/system-360. Accessed: 2024-03-09.

Jacovskis, 2011. Jacovskis, P. M. (2011). Un lugar para clementina : el Instituto de Cálculo entre 1957 y 1966. *La mensula*, 5(13). Accessed: 2024-03-09.

Lazowska, 2024. Lazowska, E. (2024). Lcm minicomputers timeline color. https://github.com/ldfaiztt/CSE451/blob/master/LCM_MinicomputersTimeline_Color_acd_CS5.pdf. Accessed: 2024-03-09.

Luisoni, 1974. Luisoni, L. (1974). Desarrollo de la Unidad Aritmetica de una mini computadora digital de propósito general. ttps://rdc.fi.uncoma.edu.ar/docs/. Accessed: 2024-03-09.

Manchester, 2024a. Manchester, U. (2024a). Ferranti Mark i. https://curation.cs.manchester.ac.uk/computer50/www.computer50.org/mark1/FM1.html. Accessed: 2024-03-09.

Manchester, 2024b. Manchester, U. (2024b). The Manchester Baby Computer. https://curation.cs.manchester.ac.uk/computer50/www.computer50.org/mark1/new.baby.html. Accessed: 2024-03-09.

Ministerio de Defensa, Dirección General de Investigación y Desarrollo, . Ministerio de Defensa, Dirección General de Investigación y Desarrollo. Mesa redonda sobre minicomputadora. Archivo Personal de Jorge Santos.

Nora and Minc, 1980. Nora, S. and Minc, A. (1980). *La informatización de la Sociedad*. Fondo de Cultura Económica.

Orbe, 2006. Orbe, P. (2006). El surgimiento y la consolidación de una universidad nueva. In Cernadas, M., editor, *Universidad Nacional del Sur: 1956-2005*, pages 77–177. EDIUNS, Bahía Blanca.

Romero et al., 2014. Romero, F., Becher, P., and Grasso, I. (2014). *En organizaciones y movimientos sociales en la historia reciente (1966-2012)*. Ediciones CEISO -IIGG.

Santos and Arango, 1957. Santos, J. and Arango, H. (1957). La operacion puente en las algebras. *Actas de las... jornadas*, 10:25.

Santos and Arango, 1970. Santos, J. and Arango, H. (1970). A graphic method for the synthesis of threshold ternary functions. *IEEE Transactions on Computers*, 100(10):975–976.

Santos La Rosa, 1973. Santos La Rosa, M. (1973). Mesa redonda sobre política nacional de computación. Centro de Estudios de Ciencias Económicas para la Liberarción Nacional, Bahía Blanca.

Santos La Rosa, 2018. Santos La Rosa, M. (2018). Historia de la educación en Bahía Blanca (1880-2001). In Cernadas, M. and Marcilese, J., editors, *Bahía Blanca siglo XX: historia política, económica y sociocultural*, pages 305–344. EDIUNS, Bahía Blanca.

UBA, 2024. UBA (2024). Historia del Departamento de Computación, Universidad de Buenos Aires. https://www.dc.uba.ar/el-departamento/#historia. Accessed: 2024-03-09.

Veitch, 1952. Veitch, E. W. (1952). A chart method for simplifying truth functions. In *Proceedings of the 1952 ACM National Meeting (Pittsburgh)*, ACM '52, page 127–133, New York, NY, USA. Association for Computing Machinery.